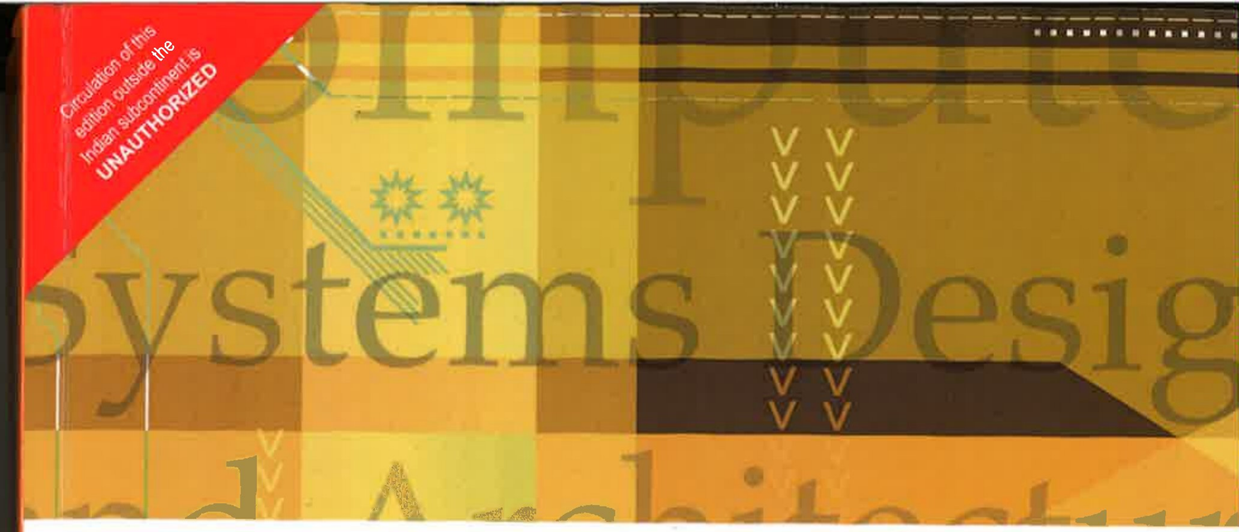

Computer Systems Design and Architecture

Second Edition

NEW! Chapters on System Software Architectures and Parallel Processing. Coverage of ARM, Blackfin and Pentium Architectures.

Vincent P. Heuring
Harry F. Jordan
T. G. Venkatesh

ALWAYS LEARNING

PEARSON

Trademark Acknowledgments

8008, 8080, 8086, Intel, Pentium, and P6 are registered trademarks of the Intel Corporation.

68000, 68010, 68020, 68040, and PPC601 are trademarks of the Motorola Corporation.

Alpha, DECnet, PDP-11, VAX, and VAX11/780 are trademarks of the Digital Equipment Corporation.

AppleTalk, LocalTalk, Macintosh, Macintosh Quadra, FireWire and QuickDraw are registered trademarks of Apple Computer, Inc.

Centronics is a registered trademark of the Centronics Data Computer Corporation.

Espresso is a registered trademark of Berkeley Systems, Inc.

FAST is a registered trademark of National Semiconductor in France, Italy, Canada, the United States, and the Benelux countries.

HPGL and PCL are registered trademarks of the Hewlett-Packard Company.

IBM, 360, and System/360 are trademarks of the International Business Machines Corporation.

Maxtor and LARAMIE are trademarks of the Maxtor Corporation.

MIPS, R3000, and R4000 MIPS are trademarks of MIPS Technology, Inc.

NetWare is a registered trademark of Novell, Inc.

NuBus is a trademark of Texas Instruments, Inc.

PostScript is a registered trademark of Adobe Systems, Inc.

SPARC and UltraSparc are registered trademarks of SPARC, International Inc., licensed to Sun Microsystems, Inc.

Tri-state is a registered trademark of National Semiconductor in member nations of the Madrid Convention.

The UNIX trademark is licensed exclusively through the X/Open Company Ltd.

VITESSE is a registered trademark of the Vitesse Semiconductor Corporation.

Windows is a registered trademark of the Microsoft Corporation.

XNS is a trademark of the Xerox Corporation.

Contents

Preface

To the Instructor

This book is suitable for an introductory course on computer design at the junior, senior, or introductory graduate level. We assume that the student has had at least an introductory course in some high-level programming language such as C or Pascal, and a semester of logic design. However, a comprehensive appendix on digital logic design, written by Professor Miles Murdocca of the Internet Institute USA, provides sufficient background material for teaching the course to students without previous digital design experience.

appendix on digital logic design

Appropriate topics for such a book have changed considerably in recent years, as desktop computers have evolved from simple, stand-alone units into complex systems attached to high-speed networks and internetworks. Earlier generations of microprocessors had almost trivial internal structure. Present designs contain multiple pipelined functional units with support for multiple processors and memories. Areas of computer design and architecture that were barely touched upon in the not-so-distant past have become major topics for discussion. Introductory compiler courses now routinely discuss optimization for pipelined processors. Users worry about whether they should add level-2 cache memory to their PCs. Support personnel wearily try to explain to the computer user how to configure the subnet mask for their network slip connection.

The topics of pipelined processor design, the memory hierarchy, and networks and internetworking are moving to center stage in the arena of computer design and architecture. Therefore we devoted the major parts of three chapters to treatment of these subjects.

pipelined processors
memory hierarchy
networking and the Internet

Given the focus on computer design and computer architecture, we approach the study of the computer from three viewpoints: the view of the assembly/machine language programmer, the view of the logic designer, and the view of the system architect.

three views of the general purpose machine

In covering the topic of gate-level computer design, we follow a model architecture through the design process, from the instruction set design level to the processor design level. Given the choice of using either a commercial machine with all of the complicating features that are necessary to make such a machine commercially successful, or using

Index

B

C

D

E

F

G

H

I

N

O

P

R

S

W

Z

Computer Systems Design and Architecture

Second Edition

Vincent P. Heuring | Harry F. Jordan | T. G. Venkatesh

Computer Systems Design and Architecture 2e places emphasis on issues related to both architecture as well as organization of the computer. It interrelates three different viewpoints to provide unique understanding of the subject: the perspectives of the logic designer, the assembly language programmer and the computer architect. The text describes both CISC and RISC models at the ISA level using the formal description language of RTN (Register Transfer Notation), allowing for an in-depth appreciation of different machine structures and functions.

Salient Features

- In-depth coverage of architectural trends such as pipelining, superscalar technique, and VLIW
- Discusses the OSI layer model and its relationship to TCP/IP Internet Protocol
- Provides thorough understanding of static and dynamic RAM design, cache memory management, virtual memory and arithmetic unit
- Detailed discussion on design of datapath and pipeline of 1, 2 and 3 bus processors
- Concepts are supplemented with practical design issues in modern processors such as Pentium, SPARC, ARM and Power PC

ISBN 978-81-775-8483-7

9 788177 584837

www.pearsoned.co.in